# CLAIMS

What is claimed is:

1. A fuse (200) for integration within a semiconductor circuit comprising: an insulating layer (205) deposited adjacent the semiconductor substrate (203); a silicon layer (201) formed a first silicon material having a first resistance deposited adjacent the insulating layer, the silicon layer having a first width; and, a metal silicide stringer (202) having a second resistance different from the first resistance deposited over a portion of the first silicon material (201) and having a second width that is less than the first width within at least a portion thereof, the metal silicide for conducting current therethrough with approximately the second resistance and for agglomerating in response to a programming current to other than conduct current therethrough with a same second resistance.

2. The fuse as recited in claim 1 wherein the silicon layer is a poly-silicon layer.

3. The fuse as recited in claim 1 wherein the silicide layer is a tungsten silicide layer.

4. The fuse as recited in claim 1 wherein the silicide layer is a platinum silicide layer.

5. The fuse as recited in claim 1 wherein the first resistance is higher than the second resistance.

6. The resistor fuse as recited in claim 1 wherein the resistor fuse forms a portion of a non-volatile multi-state memory cell.

7. The resistor fuse as recited in claim 6 wherein the memory cell is one-time programmable.

8. The resistor fuse as recited in claim 1 wherein the insulating layer comprises an oxide layer.

9. A method of manufacturing a silicided polysilicon fuse (200) comprising the steps of: depositing an insulating layer (205) on a semiconductor substrate (203); depositing polysilicon (201) adjacent the insulating layer; forming a silicide protection layer (206) adjacent the polysilicon; removing a portion of the silicide protection layer to reveal polysilicon therebelow; providing a mask for masking other than the revealed polysilicon; aligning the mask with the semiconductor substrate; and, forming a metal silicide layer adjacent (202) the revealed polysilicon, the metal silicide layer for forming a conductive path along a length thereof.

10. A method according to claim 9 comprising the step of providing electrical contacts on opposite sides of the length of the metal silicide layer (204a, 205b).

11. A method according to claim 9 wherein the insulating layer comprises an oxide layer.

12. A method according to claim 9 wherein the polysilicon layer is patterned.

13. A method according to claim 9 wherein the step of forming a silicide protection layer is performed by depositing a silicide protection layer on the polysilicon.

14. A method according to claim 9 wherein the step of forming a silicide protection layer is performed by reacting at least a chemical with the polysilicon.

15. A method according to claim 9 wherein the step of removing a portion of the silicide protection layer comprises a step of etching a portion of the silicide protection layer.

16. A method according to claim 9 forming a metal silicide layer comprises a step of: depositing a metal silicide adjacent the revealed polysilicon.

17. A method according to claim 9 forming a metal silicide layer comprises a step of: reacting at least a chemical including a metal with the revealed polysilicon.

18. A method of manufacturing a fuse comprising the steps of: providing a silicon feature of at least a minimum line width, the minimum line width dependent upon a minimum line width of a stepper tool; and, providing a fusible metal silicide stringer having a low resistance and having a stringer width substantially less than the minimum line width of the stepper tool.

19. A method according to claim 18 wherein the width of the fusible metal silicide stringer is dependent upon the mask alignment tolerance of a stepper tool.

20. A method according to claim 18 wherein the fusible metal silicide stringer is formed using a masking process.

21. An integrated circuit having a minimum line width and including a stringer fuse having a low resistance metal silicide stringer width substantially less than the minimum line width.